

RT/duroid[®] 5880LZ High Frequency Laminates Fabrication Guidelines

Material Description: RT/duroid[®] 5880LZ filled PTFE composites are ideal for use in weight-sensitive high performance applications. The laminate material is compatible with manufacturing processes for double-sided and multi-layer circuits and has a low Z-axis CTE that contributes to long-term reliability of plated-through holes.

These guidelines were developed to provide fabricators with basic information on processing stripline assemblies and multilayer boards using copper clad RT/duroid 5880LZ laminates. A Rogers' technical service or sales representative should be contacted for more detailed information pertaining especially to dimensional movement and plated through hole processing.

Storage: RT/duroid 5880LZ cores can be stored indefinitely at ambient conditions. A FIFO inventory system is recommended as is a method of record keeping that would allow tracking of material lot numbers through PWB processing and delivery of finished circuits.

INNER LAYER PREPARATION:

Tooling: RT/duroid 5880LZ is compatible with many tooling systems. Choosing whether to use round or slotted pins, external or internal pinning, standard or multiline tooling, and pre- vs. post-etch punching would depend upon the capabilities and preferences of the circuit facility and the final registration requirements. In general, slotted pins, a multiline tooling format, and post-etch punching will meet most needs. Whichever approach is used, it is good practice to retain copper around tooling holes.

A flow pattern compatible with the chosen adhesive system can be used between circuits and around the perimeter of the panel. But, in general, registration of layers (especially thin cores) is improved by retaining as much copper as possible.

Surface Preparation for Photoresist Application: A chemical process consisting of organic cleaners and a microetch is the preferred method of preparing copper surfaces for coating with liquid or film photoresist. A conveyorized spray system using an abrasive substance suspended in solution can be used to prepare copper surfaces at the slight risk of some registration control. Mechanical scrubbing should be considered for thick cores (0.060"+) only and, even then, should be performed at reduced pressures to minimize distorting the thin laminate or imparting deep scratches that change the functional spacing between copper planes.

Photoresist Application: Liquid or dry film photoresist can be applied using traditional dip or spray coating, screening, or roll lamination processes.

DES Processing: Developers, strippers, and copper etchants used to process epoxy glass materials will also work with RT/duroid 5880LZ. The ceramic filled material may require more stringent rinse & bake processing depending upon the next step in the process sequence.

Oxide Treatment: RT/duroid 5880LZ is compatible with most oxide and oxide alternative processes. It is best to use the process recommended by the supplier of the adhesive system chosen to bond together the multilayer board.

BONDING:

Final Preparation: Special pretreatments of etched surfaces using sodium or plasma processes shouldn't be necessary providing care was taken to protect the substrate surface after copper etch. Inner-layers should be baked at 120-150°C (248-302°F) for 30-120 minutes to ensure removal of volatile substances prior to MLB bonding.

Guidelines for the oxide treatment should be referenced to make certain the dry bake doesn't degrade the bond-enhancing surface.

Multilayer Adhesive System: RT/duroid 5880LZ materials are compatible with a broad range of thermosetting (FR-4, Rogers 2929, RO4400[™], etc.) and thermoplastic (3001 Bonding Film, FEP, PFA, PTFE, etc.) adhesive systems. Many factors, such as electrical performance, flow characteristics, ease of processing, and bond temperature requirements are considered when making the best overall choice. Rogers' Technical Service Engineers (TSE's) understand the trade-offs and, if asked, will help in the selection process.

Multilayer Bond Cycle: The press cycle is determined by the requirements of the chosen adhesive system. Cooling under pressure is required when using thermoplastic (meltable) films.

PTH AND OUTER LAYER/DOUBLE-SIDED CIRCUIT PROCESSING:

Drilling: Multi-layers are most commonly drilled in stacks of one. Phenolic composite boards are recommended for entry (0.010" to 0.030" thick) and exit (>0.060") layers. Sheeted aluminum and metal coated phenolic boards can also be used as entry layers.

New carbide drills are highly recommended. Standard or undercut styles can be used. Recommended chip loads (0.001" to 0.003" per revolution) and surface speeds (150 to 300 SFM) vary with tool diameter with slower infeeds and speeds being associated with finer diameter drills. Retract rate when drilling multilayer boards should be between 300 and 500 IPM and be 700 to 1000 IPM when drilling double-sided constructions. Below is a quick reference table that provides recommended parameters for commonly used drill diameters.

Tool life should be based upon inspection of cross-sectioned holes. The "twelve inch rule," which suggests changing a tool after drilling 12" of substrate, is a good place to start when setting tool life. For example, initial hit count when drilling a 0.060" thick board would be 12"/0.060" = 200 holes.

| Tool Size | | Spindle Speed Infeed | Retract | | | |
|-----------|------|-------------------------|---------|---------|-------|---------|
| (in) | (mm) | (RPM) | (IPM) | (m/min) | (IPM) | (m/min) |
| 0.0079 | 0.20 | 72500 | 72.5 | 1.8 | 300 | 7.6 |
| 0.0098 | 0.25 | 68200 | 88.7 | 2.3 | 300 | 7.6 |
| 0.0138 | 0.50 | 55400 | 83.1 | 2.1 | 300 | 7.6 |
| 0.0197 | 0.50 | 37200 | 96.4 | 2.4 | 400 | 10.2 |
| 0.0256 | 0.65 | 37200 | 74.2 | 1.9 | 400 | 10.2 |
| 0.0295 | 0.75 | 32200 | 64.4 | 1.6 | 400 | 10.2 |
| 0.0394 | 1.00 | 24100 | 48.2 | 1.2 | 400 | 10.2 |
| 0.0492 | 1.25 | 20000 | 40.0 | 1.0 | 400 | 10.2 |
| 0.0625 | 1.59 | 20000 | 40.0 | 1.0 | 400 | 10.2 |
| 0.1250 | 3.18 | 20000 | 40.0 | 1.0 | 400 | 10.2 |

Deburring: The use of flat, rigid entry materials, conservative drilling parameters, and limited hit counts with new drills should minimize the risk of copper burring. When drilled properly, cores should be ready for subsequent processing. If debur is necessary, a chemical microetch process is preferred. If mechanical processing is required, a hand pumice scrub is preferred over a suspended abrasive spray system which, in turn, is preferred over a conveyorized mechanical debur or planarization process.

Hole Preparation: Loosely deposited debris in the holes can be removed using a vapor or hydro-honing process. These processes involve directing water suspended abrasive particles through drilled holes. The soft

laminates must be properly supported through these processes.

Depending upon the adhesive system used to bond multi-layer boards, a chemical or plasma desmear process may be required. These desmear processes will have little effect on the RT/duroid 5880LZ materials and should be done prior to activation of the PTFE surface. The chemical process appropriate for desmear of the adhesive system can be used.

CF4/O2 plasma can also be used. A dual plasma cycle to accomplish desmear of an adhesive system and activation of the PTFE surface is made possible by adding the desmear cycle outlined below to the front end of the treatment cycle described in the treatment portion of this section.

| Frequency: | 40 KHz | | | |
|---------------------------------|-------------------------|--|--|--|
| Voltage: | 500-600V | | | |
| Power: | 4000-5000 Watts | | | |
| Pre-heat to 60°C (140°F) using: | | | | |
| Gases: | 90% O2, 10% N2 | | | |
| Pressure | 250 mTORR | | | |
| Desmear using: | | | | |
| Gases: | 75% O2, 15% CF4, 10% N2 | | | |
| Pressure: | 250 mTORR | | | |
| Time: | 10-30 minutes | | | |

Drilled holes in PTFE-based laminates must be treated prior to the deposition of a conductive seed layer (e.g. electroless copper or direct metallization). Not performing a surface activation treatment will most likely result in poor metal adhesion or plated voids. Two common pre-treatments for PTFE materials are sodium treatment and plasma treatment. Either can be used for treating RT/duroid 5880LZ materials.

Sources for sodium treatment chemicals:

FluoroEtch[®] Etchant

Acton Technologies, Inc, 100 Thompson St. Pittston, PA 18640. #570-654-0612

W.L. Gore Tetra-Etch® etchant 500 ML available from R.S. Hughes Company, Inc 1162 Sonora Court, Sunnyvale, CA 94086. #408 739 3211

Sources for sodium treatment services:

FluoroEtch Etchant

Acton Technologies, Inc, 100 Thompson St., Pittston, PA 18640, #570-654-0612

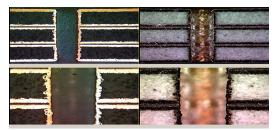
G & S Associates 1865 Sampson Ave., Corona, CA 92879 http://www.gsassociates.com, #951 739 7513

A recommended plasma cycle for treating PTFE materials is:

| Gases: | 70/30 or 80/20 H2/N2, NH3, N2, or He | |
|-------------|--------------------------------------|--|
| Pressure: | : 100 mTORR pumpdown | |
| | 250 mTORR operating | |
| Power: | 4000 Watts | |
| Frequency: | 40 KHz | |
| Voltage | 500-600V | |
| Cycle time: | 10-30 minutes | |

Metallization: RT/duroid 5880LZ materials are compatible with traditional electroless copper and direct deposit metallization processes. Cores should be baked (30-90 minutes @ 120-150°C [248-302°F]) prior to metal deposition unless plasma, which also serves as a vacuum bake, was used to prepare the hole walls for plating. A flash plate build-up of 0.0001" to 0.0003" (0.0025mm-0.0076mm) of copper is recommended to better support hole wall through preparation for outer-layer processing.

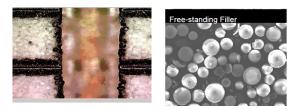
The closed microspheres, which are required to define the electrical and thermal-mechanical characteristics of RT/duroid 5880LZ laminate, result in unique wall structures of PTHs. Images of "typical" hole walls are provided below:



PTH Plating and Outer-Layer Imaging: Standard equipment and chemical processes are used to plate, image, and etch circuit patterns onto RT/duroid 5880LZ materials. Care should be taken to preserve the post-etch laminate surface. The topography that remains after copper removal promotes improved adhesion to solder masks. Materials should be rinsed and baked prior to solder mask application. Rinsing in warm or hot water for 20-30 minutes followed by 60 minutes at 125°C (257°F) should be sufficient, especially if the bake is done under vacuum.

Microspheres located at hole walls my be pierced during drill. In such cases, the inner-diameter of the hollow filler particle will define the hole

wall roughness. Punctured particles are expected to plate with copper and, in extreme examples, may plate closed. These phenomena are expected as they result from the use of the filler type that defines the unique electrical and density characteristics of the RT/duroid 5880LZ composite material. Similarly, microspheres located at the surface of cores may be fractured during after-etch PWB processing. Spheres that are open to the surface may require more stringent rinsing to avoid staining.



Final Surfaces: RT/duroid 5880LZ materials are compatible with most LPI solder masks. Epoxy solder masks are preferred if the application requires selective silk screening. Most final metal surfaces (ENIG, Sn, Ag, Ni/Au, OSP, etc.) can be applied without special issue or consideration. A bake, as was described prior to solder mask application, should be performed prior to HASL or reflow exposures.

Final Circuitization: Individual circuits can be routed, punched, or lased depending upon preference, tolerances, and edge quality requirements. Parameters for routing are provided below:

| Chip Load: | 0.00125" to 0.00250"/rev | |
|------------------------------|---|--|
| | 32mm – 64 mm/rev | |
| Speed: | 200-300 sfm | |
| | 61-92 m/min | |
| Peripheries: | Conventional cut | |
| Internal cutouts: | Climb cut | |
| Tool type: | Carbide double fluted spiral-up endmill | |
| Exit/Entry: | Phenolic or composite board | |
| Tool life: 20-30 linear feet | | |
| | 6-9 meters | |

Pre-rout vacuum channels in backer board

Double pass (opposite directions) when cleanest edge quality is required

The information in this fabrication guideline is intended to assist you in designing with Rogers' circuit materials. It is not intended to and does not create any warranties express or implied, including any warranty of merchantability or fitness for a particular purpose or that the results shown on this fabrication guideline will be achieved by a user for a particular purpose. The user should determine the suitability of Rogers' circuit materials for each application.

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